First Hit Fwd Refs

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L2: Entry 8 of 68 File: USPT Apr 17, 2001

DOCUMENT-IDENTIFIER: US 6219107 B1
TITLE: Automatic AGC bias voltage calibration in a video decoder

Application Filing Date (1):
19980824

Brief Summary Text (13):
An advantage is that the calibration feature is automatically controlled using a microprocessor. Another advantage is that performing calibration of bias voltage in the AGC circuit after acquisition of a lock to the horizontal sync, compensates for any error in the internal voltage reference and DAC output, resulting in yield enhancement.

Current US Original Classification (1):
348/678

Current US Cross Reference Classification (1):
348/572

Current US Cross Reference Classification (2):
348/689

h e b b cg b cc e

delayed by k horizontal scanning intervals (25). The comparator outputs are 01D gated (30) and the result controls a switch (21) at the output terminal (31).

ADVANTAGE - The correlation error is detected directly from carrier chrominance signal rather than from luminance signal component of playback signal.
ABSTRACTED-PUB-NO:

EP 293188A
EQUIVALENT-ABSTRACTS:

The filter circuit includes a first comb filter (20) which has a delay circuit (18) and subtractor circuit (19).

The filter acts to suppress crosstalk components from adjacent tracks contained in the playback carrier chrominance signal.

The delay time of the delay circuit is equal to ktimes the horizontal scanning interval, where k is one for NTSC system and two for PAL system. A second comb filter (24) for the playback carrier chrominance signal detects the amount of lone cor

EP 293188B

A playback chrominance signal processing circuit for processing an input playback video signal which has been reproduced from a recording medium and includes an input playback carrier chrominance signal, including processing means (12, 14) for removing noise contained in said input playback carrier chrominance signal, and line correlation error detection means (13) for detecting a degree of line correlation error between successive scan lines of said video signal, with operating characteristics of said processing means (12, 14) being controlled in accordance with said amount of line correlation error, characterised in that said line correlation error detection means (13) comprises: line correlation error detection means (13, 18, 22, 23, 24, 33, 40) coupled to receive said input playback carrier chrominance signal, for detecting an amount of line correlation error between said input playback carrier chrominance signal as currently received and said input playback carrier chrominance signal after having been delayed by an amount equal to 2k times said horizontal scanning interval, where k is a positive integer equal to one in the case of an NTSC standard playback chrominance signal and equal to two in the case of a PAL standard playback chrominance signal, and for producing a detection signal in accordance with said amount of line correlation error; and wherein said processing means comprises; filter processing means (12, 14, 18-21, 37, 38) controlled, when an amount of line correlation error of said input playback carrier chrominance signal is below a predetermined value as indicated by said detection signal, for delaying said input playback carrier chrominance signal by a time amount equal to k times the duration of a horizontal scanning interval of said video signal, to obtain a delayed playback carrier chrominance signal, and for mixing said input playback carrier chrominance signal with said delayed playback carrier chrominance signal, and controlled, when said amount of line correlation error is above said predetermined value as indicated by said detection signal, for directly outputting said input playback carrier chrominance signal as said output playback carrier chrominance signal.

CHOSEN-DRAWING: Dwg.3/9 Dwg.3/9

TITLE-TERMS: PLAYBACK CHROMINANCE SIGNAL PROCESS CIRCUIT VTR TRANSFER SIGNAL THROUGH CROSS=TALK SUPPRESS COMB FILTER ACCORD DETECT LINE CORRELATE ERROR CARRY CHROMINANCE SIGNAL

DERWENT-CLASS: W04

EPI-CODES: W04-B10; W04-F01;

SECONDARY-ACC-NO:
Non-CPI Secondary Accession Numbers: N1988-257600

L2: Entry 68 of 68 File: USPT Jul 20, 1971

DOCUMENT-IDENTIFIER: US 3594498 A
TITLE: COLOR-PHASE-CORRECTING CIRCUITRY WITH ONE-HUNDRED EIGHTY DEGREE AMBIGUITY ELIMINATION

Application Filing Date (1):
19691009

Detailed Description Text (17):
Thus, in summary, the phase comparator 20 senses whether the tape machine 10 has locked correctly to the horizontal synchronizing pulses by comparing its horizontal synchronizing pulses with the locally generated station reference signal by detecting the half subcarrier period error in the horizontal synchronizing pulse of the composite color signal. If this error is present, the phase comparator 20 will cause vertical synchronizing pulses to the tape machine slightly faster than the reference pulses until the entire signal has been shifted by one frame. The machine is allowed to relock. As the output of the tape machine 10 is not timed correctly with the editing equipment (not shown) on, the machine runs up with it off, and then the phase comparator 20 turns it on via an output signal on line 25 when it has sensed the locked condition.

Current US Cross Reference Classification (1):
348/505

L4: Entry 22 of 28 File: USPT Apr 15, 1975

DOCUMENT-IDENTIFIER: US 3878557 A
TITLE: Color framing videotape recording apparatus and method

Application Filing Date (1):
19740315

Brief Summary Text (9):
Second, with regard to time base correctors, a typical correction scheme in a color VTR includes two variable delay lines in series to remove residual time base errors still present despite a horizontal locking of the VTR servo systems. The first delay line is controlled by an error signal derived by comparison of off-tape to the input video horizontal sync pulses. The input video signal is the signal which is to be edited into material previously recorded on the tape. In most circumstances the input video signal will have a highly stable horizontal sync and color burst and the phase relation between sync and burst, whatever it may be, remains stable. The second delay line provides a fine correction under the control of an error signal comparing off-tape burst to a subcarrier derived from the input video signal. As will be explained, it is this last correction that causes color editing problems.

Detailed Description Text (108):
It will be appreciated that as part of the edit line-up procedure that a tach lock of the scanner servo is achieved followed by a horizontal lock of the VTR scanner servo. Following the achieving of horizontal lock a test edit is made by placing the machine into the edit record mode. It will be recalled from the discussion of FIGS. 10 through 13 in particular that the horizontal error is stored so that the machine timing during edit record is maintained to be the same as that during edit playback, thereby maintaining the correct timing with the possible exception of having chosen the incorrect color frame. The tape is then rewound as necessary and played back to determine if there is an abrupt 180.degree. phase shift of the color subcarrier at the edit point. As mentioned above, such a phase shift causes a noticeable shifting in the picture. If no shift was noted, then the circuitry of FIGS. 15 and 16 is properly set up so that the VTR will always lock to the correct color frame so long as the horizontal sync to color burst phase of the input video signal remains substantially constant. In the event that the incorrect color frame was locked to the circuitry of FIGS. 15 and 16 is adjusted so that the opposite phase of the color frame pulses will be chosen.

L2: Entry 28 of 68 File: USPT Dec 12, 1995

DOCUMENT-IDENTIFIER: US 5475440 A
TITLE: Digital time base corrector for video signal reproduction

Application Filing Date (1):
19931014

Detailed Description Text (7):
The switching control circuit 25 is made up of seven D-type flip-flops 26 to 32, AND circuits 33 and 34, and an NOR circuit 35. That is, a burst error holding signal is supplied to a D input terminal of the flip-flop 26. A Q output terminal of the flip-flop 26 is connected to a D input terminal of the flip-flop 27 and to one input terminal of the AND circuit 33 of two inputs. A Q output terminal of the flip-flop 27 is connected to another input terminal of the AND circuit 33. A track jump signal is supplied from a tracking servo system to a D input terminal of the flip-flop 28. A horizontal lock signal which is obtained from the loop circuit in the error calculating circuit 17 is supplied to a D input terminal of the flip-flop 29. The horizontal lock signal indicates that the PLL loop circuit to form the horizontal sync error signal is locked.

Detailed Description Text (15):
When the horizontal sync error signal or the burst error signal should be held, the error holding signal is set to the high level. When there is no need to hold the horizontal sync error signal or the burst error signal, the error holding signal is set to the low level. The track jump signal is set to the high level in a state in which the tracking servo loop is open. The track jump signal is set to the low level when the tracking servo loop is closed. When the horizontal loop circuit in the error calculating circuit 17 is in a locking state, the horizontal lock signal is set to the high level. When it is in an unlocking state, the horizontal lock signal is set to the low level. When the 1H clock signal is supplied to the D-type flip-flops 26 to 32, the input level of the input terminal D is transmitted to a Q output terminal, so that the outputs of the flip-flops 26, 28, and 29 correspond to the new input level every 1H period of timer.

Detailed Description Text (17):
Therefore, when the above conditions continue for 3H or longer, the output level of the AND circuit 34 is set to the high level and is supplied to the switch SW1. When the output level of the AND circuit 34 is at the low level, the switch SW1 is set into a selecting state of the output side of the horizontal sync error forming circuit 12. When the output level of the AND circuit 34 is at the high level, the switch SW1 is set to a selecting state on the output side of the burst error forming circuit 11. When the horizontal loop circuit is in the locking state and the horizontal lock signal is at the high level and the period signal is at the high level for the generating period of time of the color burst signal and the horizontal sync signal of the reproduction video signal, the output level of the AND circuit 37 is set to the high level, so that the switch SW2 is turned off. In the other cases, the switch SW2 is turned on.

Detailed Description Text (18):
When the output level of the AND circuit 34 is at the low level and the switching conditions of the switch SW1 are not satisfied, the horizontal sync error signal is

relayed by the switch SW1. Therefore, the frequency of the oscillation signal of the VCO 22 is set to a value in accordance with the horizontal sync error signal. The oscillation signal is supplied to the write control circuit 6 through the phase shifter 23, thereby deciding the generating timing of the write clock signal WCLK. In this instance, when the horizontal loop circuit is in a locking state and lies within the burst signal period of time or horizontal sync signal period of time, the switch SW2 is turned off, so that the phase of the oscillation signal is unchanged without being shifted by the phase shifter 23. When the horizontal loop circuit is in an unlocking state or doesn't lie within both of the burst signal period of time and the horizontal sync signal period of time, the switch SW2 is turned on, so that the phase of the oscillation signal is shifted by the phase shifter 23 in accordance with the gain-adjusted horizontal sync error signal, thereby executing the phase modulation.

Detailed Description Text (19):
When there is no need to hold the burst error signal and a state in which the tracking servo loop is in a closed state and, further, the horizontal loop circuit is in a locking state continues for a time interval of 3H or longer, the switching conditions of the switch SW1 are satisfied and the switch SW1 is switched to the selecting state of the output side of the burst error forming circuit 11 in accordance with the high level output of the AND circuit 34. Since the burst error signal is relayed by the switch SW1, the frequency of the oscillation signal of the VCO 22 is set to a value according to the burst error signal. The oscillation signal is supplied to the write control circuit 6 through the phase shifter 23, thereby deciding the generating timing of the write clock signal WCLK. In this instance, when the horizontal loop circuit is in a locking state and lies within the burst signal period of time or the horizontal sync signal period of time, the switch SW2 is turned off, so that the phase of the oscillation signal is unchanged without being shifted by the phase shifter 23. When the horizontal loop circuit lies within none of the burst signal period Of time and the horizontal sync signal period of time, the switch SW2 is turned on, so that the phase of the oscillation signal is shifted by the phase shifter 23 in accordance with the gain adjusted horizontal sync error signal, thereby performing the phase modulation.

Current US Original Classification (1):
348/498

Current US Cross Reference Classification (1):
348/497

Current US Cross Reference Classification (2):
348/536

Current US Cross Reference Classification (3):
348/537

Current US Cross Reference Classification (4):
348/540

Current US Cross Reference Classification (5):
348/549

CLAIMS:

1. A digital time base corrector comprising:

A/D converting means for converting a reproduced video signal read out and reproduced from a recording medium into a digital signal;

memory control means for writing said digital signal into an image memory in

accordance with a write clock signal and for reading out said digital signal from said image memory in accordance with a read clock signal of a predetermined period of time;

D/A converting means for converting said read-out digital signal into an analog video signal,

wherein said memory control means comprises

clock forming means for forming a sync clock signal having a phase synchronized with a time base fluctuation included in said reproduced video signal in accordance with at least one of a horizontal sync signal and a color burst signal which are separated from said reproduction video signal, and

modulating means for obtaining said write clock signal by phase modulation of said sync clock signal in accordance with a burst error signal indicative of a time base fluctuation of said color burst signal in a period of time other than a period in which at least said color burst signal in said reproduced video signal is generated; and

switching relay means for selectively relaying one of a burst error signal and a horizontal sync error signal to said clock forming means in accordance with a burst error hold signal and a horizontal lock signal.

2. A digital time base corrector according to claim 1, wherein said switching relay means relays one of the burst error signal and the horizontal sync error signal to said clock forming means in accordance with the burst error hold signal, the horizontal lock signal, and a track jump signal.

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L2: Entry 22 of 68 File: USPT Mar 11, 1997

DOCUMENT-IDENTIFIER: US 5610667 A
** See image for Certificate of Correction **
TITLE: Apparatus and method for maintaining synchronism between a picture signal and a matrix scanned array

Application Filing Date (1):
19950824

Detailed Description Text (38):
More importantly, when the phase locked loop 108 is not locked to the NTSC composite signal NTSC.sub.-- COMP, the horizontal sync detector 180 of FIG. 6 allows greater than 50% of the composite sync signal COMP.sub.-- SYNC to be provided as the horizontal sync signal HORZ.sub.-- SYNC to the phase locked loop. Consequently, the phase locked loop 108 has a better likelihood of receiving rising edges of the composite sync signal COMP.sub.-- SYNC during each horizontal line, but before lock, with the horizontal sync detector 180 than with the horizontal sync detector 104. Therefore, the horizontal sync detector 180 allows the phase comparator 110 to generate an appropriate error signal during each horizontal line (rather than, for example, detecting an edge every several horizontal lines). Consequently, the horizontal sync detector 180 allows the phase locked loop 108 to lock to the incoming composite sync signal COMP.sub.-- SYNC.

Detailed Description Text (39):
Once the phase locked loop 108 is locked, the horizontal sync detector 180 of FIG. 6 enables portions of the composite sync signal COMP.sub.-- SYNC to be passed near the beginning of a horizontal line as the horizontal sync signal HORZ.sub.-- SYNC and disables or does not pass the signal near the beginning of the next horizontal line, as with the horizontal sync detector 104 of FIG. 5. As a result, the horizontal sync detector 180 passes the horizontal sync pulses 131, 132, 133, etc. during the active lines of video, and passes the first of each pair of equalizing pulses or vertical sync pulses occurring during each horizontal line in the vertical blanking interval 147. The phase comparator 110 thereby receives a well-behaved horizontal sync signal HORZ.sub.-- SYNC that has a single frequency.

Detailed Description Text (45):
In this way, the horizontal sync detector 204 allows the phase locked loop 108 to receive a "high" value pulse after receiving the pointer signal B, produce an error signal, and quickly lock to the COMP.sub.-- SYNC signal. Once the phase locked loop 108 is locked, the horizontal sync detector 204 enables portions of the composite sync signal COMP.sub.-- SYNC to be passed near the beginning of the horizontal line as the horizontal sync signal HORZ.sub.-- SYNC, and disables or does not pass the COMP.sub.-- SYNC signal near the beginning of the next horizontal line, as with the horizontal sync detector 104 of FIG. 5. As a result, the horizontal sync detector 204 passes the horizontal sync pulses 131, 132, 133, etc. during the active lines of video, and passes the first of each pair of equalizing pulses or vertical sync pulses occurring during each horizontal line and the vertical blanking interval 147. The phase comparator 110 thereby receives a well-behaved horizontal sync signal HORZ.sub.-- SYNC that has a single frequency.

Current US Original Classification (1):

h e b b cg b cc e

348/796

Current US Cross Reference Classification (3):
348/531

Current US Cross Reference Classification (4):
348/540

h e b b cg b cc e

First Hit Fwd Refs

Generate Collection Print

L2: Entry 10 of 68 File: USPT Mar 14, 2000

DOCUMENT-IDENTIFIER: US 6037994 A
TITLE: Sync signal processing device for combined video appliance

Application Filing Date (1):
19970509

Brief Summary Text (10):
The sync signal processing circuit 2 is provided with a horizontal sync separating section 6 for separating the horizontal sync signal Hsync inputted from the video processing section 1, a horizontal locking section 7 for locking the horizontal sync signal outputted from the horizontal sync separating section 5 into a horizontal blanking section 8 for processing a horizontal blanking in compliance with a, input horizontal deflection pulse signal, a phase detecting section 9 for detecting the phase of the horizontal sync signal provided from the horizontal sync separating section 6, an oscillation section 10 for oscillating with a frequency of 503.5 KHz in accordance with the output of the phase detecting section 9, a divider 11 for dividing by 32 the output of the oscillation section 10 and providing the divided frequency to the phase detecting section 9 to achieve a phase locked loop (PLL), a phase detecting section 12 for detecting the phase of the output of the divider 11 and the output of the horizontal blanking section 9, a phase shifting section 13 for shifting the output of the phase detecting section 12, a horizontal driving section 14 for providing to the horizontal output circuit 3 the horizontal driving signal HD in accordance with the output of the phase shifting section 13, a phase detecting section 15 for detecting the phase of the output of the divider 11, an oscillation section 16 for oscillating with a frequency of 16 MHz in accordance with the output of the phase detecting section 15, and a divider 17 for dividing by 1024 the output of the oscillation section 16 and providing the divided frequency to the phase detecting section 15 to achieve a PLL.

Brief Summary Text (13):
The horizontal sync separating section 6 separates the horizontal sync signal form the input video signal, and the horizontal locking section 7 is locked into the horizontal deflection pulse signal inputted to the horizontal blanking section 8. The horizontal blanking section 8 performs the horizontal blanking process of the inputted horizontal deflection pulse signal and provides the processed signal to the horizontal locking section 7, phase detecting section 12, and the count-down processor 19.

Current US Original Classification (1):
348/510

Current US Cross Reference Classification (2):
348/500

Current US Cross Reference Classification (3):
348/516

Current US Cross Reference Classification (4):
348/521

h e b b cg b cc e

Current US Cross Reference Classification (5):
348/525

Current US Cross Reference Classification (6):
348/542

Current US Cross Reference Classification (7):
348/554

h e b b cg b cc e

DOCUMENT-IDENTIFIER: US 5347365 A
TITLE: Device for receiving closed captioned broadcasts

Application Filing Date (1):
19920922

Brief Summary Text (19):
According to a feature of the invention, there is provided a device for receiving and decoding closed caption broadcasting data multiplexed within a television signal and displaying character information contained in the data on a television screen, comprising: a synchronizing/separator circuit for separating a horizontal synchronizing signal and a vertical synchronizing signal contained within the television signal, an automatic frequency control circuit, the automatic frequency control circuit including a voltage controlled oscillator, means for charging and discharging a capacitor from a constant current source, an output frequency of the voltage controlled oscillator being controlled by a charging and discharging rate of the capacitor, a first phase comparator, the first phase comparator receiving the horizontal synchronizing signal and an output of the output frequency, and including means for producing an error signal in response to differences in its inputs, a low pass filter receiving the error signal and effective to produce a filtered error signal, the automatic frequency control circuit being responsive to the filtered error signal for locking the output and the horizontal synchronizing signal in phase, means for sampling a run-in clock signal encoded within the television signal, a second phase comparator for phase-comparing the sampled run-in clock signal with an output signal of the voltage controlled oscillator, and a control circuit for varying the voltage controlled oscillator output signal according to an output signal of the second phase comparator.

Current US Original Classification (1):
348/525

Current US Cross Reference Classification (3):
348/476

Current US Cross Reference Classification (4):
348/540

CLAIMS:

4. A device for receiving and decoding closed caption broadcasting data multiplexed within a television signal and displaying character information contained in said data on a television screen, comprising:

a synchronizing/separator circuit for separating a horizontal synchronizing signal and a vertical synchronizing signal contained within said television signal;

an automatic frequency control circuit;

said automatic frequency control circuit including a voltage controlled oscillator having means for charging and discharging a capacitor from current sources;

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an output frequency of said voltage controlled oscillator being controlled by a charging and discharging rate of said capacitor;

a first phase comparator;

said first phase comparator receiving said horizontal synchronizing signal and an output of said voltage controlled oscillator at said output frequency, and including means for producing an error signal in response to differences in its inputs;

a low pass filter receiving said error signal and producing a filtered error signal;

said automatic frequency control circuit being responsive to said filtered error signal for locking said output and said horizontal synchronizing signal in phase;

means for extracting a run-in clock signal encoded within said television signal;

a second phase comparator for phase-comparing said extracted run-in clock signal with an output signal of said voltage controlled oscillator;

a control circuit for varying said voltage controlled oscillator output signal, via said means for charging and discharging, according to an output signal of said second phase comparator such that said output frequency is varied so as to track a frequency of said run-in signal; and

a decoder circuit for decoding said caption data responsive to said output signal of said voltage controlled oscillator.

L2: Entry 31 of 68 File: USPT Sep 13, 1994

DOCUMENT-IDENTIFIER: US 5347365 A
TITLE: Device for receiving closed captioned broadcasts

Application Filing Date (1):
19920922

Brief Summary Text (19):
According to a feature of the invention, there is provided a device for receiving and decoding closed caption broadcasting data multiplexed within a television signal and displaying character information contained in the data on a television screen, comprising: a synchronizing/separator circuit for separating a horizontal synchronizing signal and a vertical synchronizing signal contained within the television signal, an automatic frequency control circuit, the automatic frequency control circuit including a voltage controlled oscillator, means for charging and discharging a capacitor from a constant current source, an output frequency of the voltage controlled oscillator being controlled by a charging and discharging rate of the capacitor, a first phase comparator, the first phase comparator receiving the horizontal synchronizing signal and an output of the output frequency, and including means for producing an error signal in response to differences in its inputs, a low pass filter receiving the error signal and effective to produce a filtered error signal, the automatic frequency control circuit being responsive to the filtered error signal for locking the output and the horizontal synchronizing signal in phase, means for sampling a run-in clock signal encoded within the television signal, a second phase comparator for phase-comparing the sampled run-in clock signal with an output signal of the voltage controlled oscillator, and a control circuit for varying the voltage controlled oscillator output signal according to an output signal of the second phase comparator.

Current US Original Classification (1):
348/525

Current US Cross Reference Classification (3):
348/476

Current US Cross Reference Classification (4):
348/540

CLAIMS:

4. A device for receiving and decoding closed caption broadcasting data multiplexed within a television signal and displaying character information contained in said data on a television screen, comprising:

a synchronizing/separator circuit for separating a horizontal synchronizing signal and a vertical synchronizing signal contained within said television signal;

an automatic frequency control circuit;

said automatic frequency control circuit including a voltage controlled oscillator having means for charging and discharging a capacitor from current sources;

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an output frequency of said voltage controlled oscillator being controlled by a charging and discharging rate of said capacitor;

a first phase comparator;

said first phase comparator receiving said horizontal synchronizing signal and an output of said voltage controlled oscillator at said output frequency, and including means for producing an error signal in response to differences in its inputs;

a low pass filter receiving said error signal and producing a filtered error signal;

said automatic frequency control circuit being responsive to said filtered error signal for locking said output and said horizontal synchronizing signal in phase;

means for extracting a run-in clock signal encoded within said television signal;

a second phase comparator for phase-comparing said extracted run-in clock signal with an output signal of said voltage controlled oscillator;

a control circuit for varying said voltage controlled oscillator output signal, via said means for charging and discharging, according to an output signal of said second phase comparator such that said output frequency is varied so as to track a frequency of said run-in signal; and

a decoder circuit for decoding said caption data responsive to said output signal of said voltage controlled oscillator.

First Hit Fwd Refs

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L2: Entry 66 of 68 File: USPT Jul 31, 1973

DOCUMENT-IDENTIFIER: US 3749826 A
TITLE: COLOR TELEVISION SIGNAL REPRODUCING SYSTEM

Application Filing Date (1):
19710511

Detailed Description Text (1):
FIG. 1 shows the principles underlying the invention. According to the invention, the recovered color signal of center frequency f.sub.S including timing error information and the horizontal sync signal at frequency f.sub.H also including timing error information, as represented by a in FIG. 1, are processed to produce a reference signal with frequency f'.sub.H, as represented by b, which is locked to phase variations in the horizontal sync signal f.sub.H. The reference signal thus obtained is used, for example, to derive the f.sub.S color signal, a frequency converted color signal having a center frequency f.sub..beta., in which the timing error component is partially or totally cancelled out.

Current US Original Classification (1):
348/502

L2: Entry 6 of 6 File: DWPI Nov 30, 1988

DERWENT-ACC-NO: 1988-339736
DERWENT-WEEK: 198848

TITLE: Playback chrominance signal processing circuit for VTR - transfers signal through cross=talk suppression comb filter according to detected line correlation error of carrier chrominance signal

PF Application Date (1):
19880525

PF Application Date (2):
19880525

PF Application Date (3):
19880525

PF Application Date (5):
19880525

PF Application Date (6):
19870525

Equivalent Abstract Text (4):
A playback chrominance signal processing circuit for processing an input playback video signal which has been reproduced from a recording medium and includes an input playback carrier chrominance signal, including processing means (12, 14) for removing noise contained in said input playback carrier chrominance signal, and line correlation error detection means (13) for detecting a degree of line correlation error between successive scan lines of said video signal, with operating characteristics of said processing means (12, 14) being controlled in accordance with said amount of line correlation error, characterised in that said line correlation error detection means (13) comprises: line correlation error detection means (13, 18, 22, 23, 24, 33, 40) coupled to receive said input playback carrier chrominance signal, for detecting an amount of line correlation error between said input playback carrier chrominance signal as currently received and said input playback carrier chrominance signal after having been delayed by an amount equal to 2k times said horizontal scanning interval, where k is a positive integer equal to one in the case of an NTSC standard playback chrominance signal and equal to two in the case of a PAL standard playback chrominance signal, and for producing a detection signal in accordance with said amount of line correlation error; and wherein said processing means comprises; filter processing means (12, 14, 18-21, 37, 38) controlled, when an amount of line correlation error of said input playback carrier chrominance signal is below a predetermined value as indicated by said detection signal, for delaying said input playback carrier chrominance signal by a time amount equal to k times the duration of a horizontal scanning interval of said video signal, to obtain a delayed playback carrier chrominance signal, and for mixing said input playback carrier chrominance signal with said delayed playback carrier chrominance signal, and controlled, when said amount of line correlation error is above said predetermined value as indicated by said detection signal, for directly outputting said input playback carrier chrominance signal as said output playback carrier chrominance signal.

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L2: Entry 6 of 6 File: DWPI Nov 30, 1988

DERWENT-ACC-NO: 1988-339736
DERWENT-WEEK: 198848

TITLE: Playback chrominance signal processing circuit for VTR - transfers signal through cross=talk suppression comb filter according to detected line correlation error of carrier chrominance signal

INVENTOR: KOSAKA, Y; YAMADA, K

PATENT-ASSIGNEE:

ASSIGNEE	CODE
VICTOR CO OF JAPAN	VICO

PRIORITY-DATA: 1987JP-0125963 (May 25, 1987)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
EP 293188 A	November 30, 1988	E	019	
DE 3872770 G	August 20, 1992		000	H04N009/79
EP 293188 B1	July 15, 1992	E	024	H04N009/79
JP 63292796 A	November 30, 1988		000	

DESIGNATED-STATES: DE FR GB DE FR GB

CITED-DOCUMENTS:DE 2911927; DE 3504647 ; EP 217565 ; FR 2502879 ; US 4658285

APPLICATION-DATA:

PUB-NO	APPL-DATE	APPL-NO	DESCRIPTOR
EP 293188A	May 25, 1988	1988EP-0304746	
DE 3872770G	May 25, 1988	1988DE-3872770	
DE 3872770G	May 25, 1988	1988EP-0304746	
DE 3872770G		EP 293188	Based on
EP 293188B1	May 25, 1988	1988EP-0304746	
JP 63292796A	May 25, 1987	1987JP-0125963	

INT-CL (IPC): H04N 5/21; H04N 9/79

ABSTRACTED-PUB-NO: DE 3872770G
BASIC-ABSTRACT:

The filter circuit includes a first comb filter (20) which has a delay circuit (18) and subtractor circuit (19). The filter acts to suppress crosstalk components from adjacent tracks contained in the playback carrier chrominance signal. The delay time of the delay circuit is equal to times the horizontal scanning interval, where k is one for NTSC system and two for PAL system.

A second comb filter (24) for the playback carrier chrominance signal detects the amount of lone correlation error between the playback chrominance signal currently being received and that signal after having been delayed by 2k horizontal scanning intervals. The line correlation error detection signal outputs are compared (27,29) from a respective full wave rectifier (26,28) of which one (26) receives the signal